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In recent years, due to the microminiaturization of such elements, the gate length of the MISFET has been made very fine and the gate insulating film has been made very thin. For example, in the adoption of a silicon oxide film thinner than 2 nm (physical film thickness) as a gate insulating film, difficulty is encountered due to its tunnel current, for example, as well as the reliability problem involved. For this reason, in place of such silicon oxide film, the adoption of a high dielectric-constant film, such as a silicon nitride film and Ta<sub>2</sub>O<sub>5</sub> film, has been studied because it can be increased in thickness.

✓ Please change the paragraph beginning at page 4, line 23, and ending on page 5, line 7, as shown in the attached marked-up copy to read as follows:

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In an example of FIG. 7, after the dummy gate electrode 115 has been removed as shown in FIG. 5 to provide a trench for a final buried type gate electrode formation, a high dielectric-constant film, such as the Ta<sub>2</sub>O<sub>5</sub>, is formed, as a gate insulating film 201, by using the chemical vapor deposition method, for example, in place of forming the above-mentioned silicon oxide film by the thermal oxidation method. The above-mentioned high dielectric-constant film, being formed by the chemical vapor deposition method and sputtering method, is formed, as shown in FIG. 7, also on the sidewall of the trench for the gate electrode formation.

✓ Please change the paragraph beginning at page 11, line 20, and ending at page 12, line 4 as shown in the attached marked-up copy to read as follows:

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After forming an isolation region 302 on a p type semiconductor substrate 301, as shown in FIG. 9, an about 5 nm-thick SiO<sub>2</sub> film 303 serving as a dummy gate insulating film is deposited by a thermal oxidation method on a surface of the substrate 301. Thereafter, an about 100 nm-thick polycrystalline silicon film 304 serving as a dummy gate electrode is deposited by a chemical vapor deposition method, for example, on the SiO<sub>2</sub> film 303.

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(concluded)

Thereafter, an about 50 nm-thick silicon nitride film 305 is stacked by the chemical vapor deposition method, for example, on the polycrystalline silicon film 304.

Please change the paragraph beginning at page 14, line 9, and ending at page 15, line 3, as shown in the attached marked-up copy to read as follows:

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Thereafter, as shown in FIG. 14, the width of the trench 312 is enlarged by an extent corresponding to the film thickness of a desired gate insulating film. In the case of using a Ta<sub>2</sub>O<sub>5</sub> film of 40 nm as the gate insulating film, an etching process is done on the sidewall surface of the trench 312 to an extent corresponding to 40 nm or more. By doing so, the trench 312 is enlarged to a trench 312' for burying a material for a final gate electrode. It is desirable to perform an etching at this time such that both the dummy gate insulating film 303 present on the bottom and sidewall insulating film 308 present on the sidewall area of the burying trench are simultaneously etched, with an adequate selectivity to the semiconductor substrate 101. In the present embodiment using an SiO<sub>2</sub> for both the dummy gate insulating film 303 and sidewall insulating film 308 and a silicon for the semiconductor substrate 101, it is effective to perform an etching using a dilute HF or dilute NH<sub>4</sub>F, for example, or an isotropic dry etching using a CDE, for example, that is, an etching having a selectivity to the substrate.

Please amend the paragraph beginning at page 16, line 2, as shown in the attached marked-up copy to read as follows:

A<sup>5</sup>  
Then, a 300 nm-thick tungsten, for example, serving as a final gate electrode 314 is deposited by the chemical vapor deposition method, sputtering method, for example, over the gate insulating film 313 on the structure shown in FIG. 15. Thereafter, a CMP polishing is done and the burying of tungsten as the gate electrode 314 in the trench 312' is completed (FIG. 16).